REMARKS

Claims 1, 2, 4-8 and 10-15 are pending. The Examiner's reconsideration of the rejections is respectfully requested in view of the amendments and remarks.

Applicants appreciate the Examiner's indication that claims 2-4 and 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 1 has been objected to, wherein the Examiner stated that it is not clear as to the recitation "the reference voltage signal" on line 8 is the same of different than the "a reference voltage" on line 4. Claim 1 has been amended to clarify the recitations. The Examiner's reconsideration of the objection is respectfully requested.

Claims 1, 5, 6, 7, and 11 have been objected to under 35 USC 102(e) as being anticipated by Cyrusian et al. (U.S. Patent No. 6,697,205). The Examiner stated essentially that Cyrusian teaches every limitation of claim 1, 5, 6, 7 and 11.

Claim 1 claims, *inter alia*, "the reference current generator comprises a first PMOS transistor comprising a source connected to a power supply voltage and a gate connected to an output terminal of the OP amp, and first to third resistors connected in series between the first PMOS transistor and the ground voltage, a voltage level between the first resistor and the second resistor being the first voltage." Claim 6 claims, *inter alia*, "the reference current generator means comprises a first field effect transistor comprising a source connected to a power supply voltage and a gate connected to an output terminal of the amplifier means, and first through third resistors connected in series between the first field effect transistor and the ground voltage, a voltage level between the first resistor and the second resistor being the first voltage."

Cyrusian teaches a temperature detection circuit operating in response to an impedance of

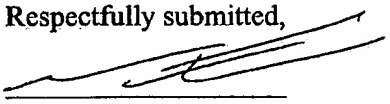
a replica transistor (308) (see Figure 3 and col. 8, lines 3-19). Cyrusian does not teach that a reference current generator comprises a first PMOS transistor comprising a source connected to a power supply voltage and a gate connected to an output terminal of the OP amp, and first to third resistors connected in series between the first PMOS transistor and the ground voltage, a voltage level between the first resistor and the second resistor being the first voltage, as claimed in claim 1 and essentially as claimed in claim 6. Claims 1 and 6 include the allowable limitations of claims 3 and 9, respectively. Accordingly, claims 1 and 6 are believed to be in condition for allowance.

Claim 5 depends from claim 1. Claims 7 and 11 depend from claim 6. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 6. The Examiner's reconsideration of the rejection is respectfully requested.

New claim 12 includes the limitations of claim 1 and allowable claim 4. Accordingly, claim 12 is believed to be in condition for allowance. Claims 13-15 depend from claim 12. Claims 13-15 are believed to be allowable for at least the reasons given for claim 12.

For the forgoing reasons, the present application, including claims 1, 2, 4-8 and 10-15, is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully urged.

Respectfully submitted,



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